

```

a = 1'b0;
b = 1'b1;
#100
a = 1'b1;
b = 1'b1;
end
endmodule

```

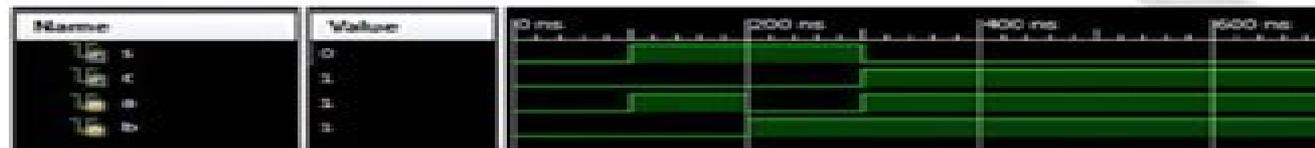


Figure 4.6 RTL Simulation waveform for code for Half adder

Step 3: Review the console output for results and debugging information.

At time 0: a=0 b=0, s=0, c=0

At time 100000: a=1 b=0, s=1, c=0

At time 200000: a=0 b=1, s=1, c=0

At time 300000: a=1 b=1, s=0, c=1

4.2.3 APPLICATIONS OF HALF ADDER:

1. Half adders are used in various digital circuits, including arithmetic logic units (ALUs) and adder-subtractor units.
2. They are the basic building blocks for constructing full adders and multi-bit adders.
3. Half adders can be used to add two binary numbers to get the least significant bits of the result.

4.3 FULL ADDER

4.3.1 THEORY

The full adder adds three single-bit input and produce two single-bit output. Thus, it is useful when an extra carry bit is available from the previously generated result.

Microprocessors Lab Manual Vtu

Michael Brown



Microprocessors Lab Manual Vtu:

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