Delay Analysis of Half Subtractor using CMOS and Pass Transistor Logic

Ishika Sharma
ME Scholar
NITTTR Chandigarh

Rajesh Mehra
Associate Professor
NITTTR Chandigarh

ABSTRACT

In present day skill, designing of low power systems has emerged as one of the vital theme of electronic industries due to the point that, power consumption is drawing much of the absorption in any very large scale integration (VLSI) chip design. Design of low power circuit for high performance is the necessary main concern of VLSI technique. This paper presents designing of Half Subtractor using basic gates which are drawn by conventional CMOS and Pass Transistor Logics based on 45nm technology . In comparison between conventional CMOS half subtractor and using Pass Transistor Logic the delay is 10.5% less in PTL's half subtractor which is due to less number of transistors used in Pass Transistor Logic which in further has reduced the transistor count to 28.57%.

Keywords
Half subtractor, pass transistor logic, digital circuits.

1. INTRODUCTION

A low-power integration need can be defined at different design levels, such as the circuit design and the process technology level. As the modern multimedia world is developing low power devices are in demand [1].Digital circuits which are designed by using conventional CMOS cannot fulfill these basic requirements so some solutions are found out and the outcome has resulted in the form of pass transistor logic [2]. In VLSI designing the rapid increase in demand for low power can be dealt at various logic levels, such as circuit, architectural and layout. At circuit design level substantial quantity of power can be saved by way of proper option of a logic manner. The proper option of a logic manner is value able because all significant constraints leading power dissipation, switching capacitance, transition motion, and short circuit currents are strongly prejudiced by the chosen logic style [3]. Indeed, designing high-speed low-power circuits with CMOS technology has been a main research problem. Numerous logic families have been planned and used to recover circuit routine outside that of conventional static CMOS family. In addition, due to technology growing the number of transistors on chip, the presentation of static CMOS circuits originates at considerable area where power dissipation value that may be critical, specifically for transportable appliances. Innovative devices that address the power and performance encounters must be therefore, explored [4]. There are a various logic methods through which a circuit can be realized. The proper choice of a logic strategy is significant because all important constraints governing power dissipation- switching capacitance, transition activity, and short circuit currents are powerfully prejudiced by the chosen logic design [5].

2. HALF SUBTRACTOR

A subtractor is combinational logic circuit which takes binary numbers as inputs and subtract one input from other input and generates their difference and borrow as outputs.

Although subtractors can be built for many binary code representations, like excess-3, gray code or even binary-coded decimal, the most public subtractors operate on binary numbers. While carrying out subtraction between the two numbers, two's complement or ones' complement is very normally used to signify the negative numbers. Also due to the affluence with which calculations are performed, many a times modifying an adder to a adder–subtraction is measured comparatively important. Other signed number representations require a more composite subtractor. Depending upon the submission of the device or upon the purpose of the application to be achieved, the inputs to the circuit device may differ from two to three. We could perhaps use an Half-Subtractor if we have two inputs though for three inputs, a Full-Subtractor can be used [6]. Basically subtractors are of two types half subtractor and full subtractor. The logic symbol and truth table are shown below in figure 1 and logic diagram is drawn in figure 2. The table 1 describes according ling the output produced.

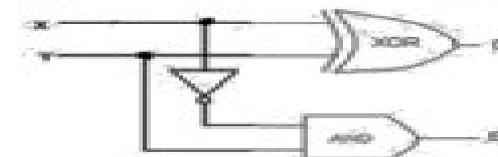Fig. 1. 1:2 Half Subtractor Block diagram

Fig 2. Logic Diagram of Conventional Half Subtractor

Table 1. Truth Table of Half Subtractor

INPUTS		OUTPUTS	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

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