

Design of a 16-bit RISC Processor Using VHDL

Karansingh P. Thakor, Ankushkumar Pal
Department of EXTC
Xavier Institute of Engineering
Mumbai, India

Prof. Madhura Shirodkar
Department of EXTC
Xavier Institute of Engineering
Mumbai, India

Abstract— This paper targets the design and implementation of a 16-bit RISC Processor using VHDL (Very High Speed Integrated Circuit Hardware Description Language). As IC chip design involves complex computations and intense usage of resources, by using an HDL we can save resources and time by implementing it using the software approach. The implementation strategies have been borrowed from the popular MIPS architecture to a certain extent. The processor has 16-bit arithmetic and logical instruction set which has been designed and simulated. The instruction set is extremely simple and it gives an insight into the kind of hardware that would be required to execute the instructions accordingly. The ALU, instruction register, program counter, register file, control unit and memory have been integrated in the proposed processor. All the modules in the design are coded in VHDL to ease the description, verification, simulation and hardware implementation. The blocks are designed using the behavioral approach.

Keywords — RISC Processor, MIPS, SPU, ALU, ISA, VHDL, PC, Opcode, clock, timing, FPGA, instruction, LEAD, JZ, JNZ, ADD, ALB, AGB, waveform, RTL Schematic, 16-bit, Xilinx ISE, Isim.

I. INTRODUCTION

Processors are divided into 3 categories 8-bits, 16-bits and 32-bits depending upon the demand of performance, cost, power and programmability. 16-bit processors have higher performance and power than 8-bit processors and lower power consumption than 32-bit processors. They are often used in 16-bit applications such as disk driver controller, cellular communication and airbags. A RISC processor uses load-store architecture, fixed length instructions and pipelining. In load-store architecture, load instruction reads data from memory and writes it to a register, data-processing instructions process data available in registers and write the result to a register and store instruction copies data from register to memory.

This paper investigates the methodology of soft-core processor development. The software used was Xilinx ISE 14.5. The target family chosen was Spartan 6 FPGA with device XC6SLX9 and package CSG324. The simulation was performed in ISim.

II. INSTRUCTION SET

The first step was to design the Instruction Set Architecture (ISA). The instruction set contains instructions supported by the processor. The first nine instructions perform arithmetic and logical instructions. The memory read instruction reads the data from the memory address which is specified in a register (Rs) and writes the data word to the register mentioned in the instruction (Rd). The memory write instruction writes the data in the specified register (Rs) to the target address which is also

specified in a register (Rt). There is an unconditional jump that jumps to a memory address that is calculated by adding the current value in the Program Counter and the 8-bit offset specified in the instruction. This gives the target branch address. A similar procedure is followed by the Conditional Jumps but the address is calculated beforehand as an optimistic operation and is stored in a special register, so that if the condition is true then the branch target address is written into the Program Counter. If the condition is false then the Program Counter will not be modified and execution will continue as if no branching took place. There is also a no operation (NOP) instruction. The complete instruction set is given in Table I.

TABLE I. INSTRUCTION SET

	Instruction	Opcode	Operation
1	ADD	0 0 0 0	$Rd = Rs1 + Rs2$
2	SUB	0 0 0 1	If $Rs1 > Rs2$ Then $Rd = Rs1 - Rs2$ Else $Rd = Rs2 - Rs1$
3	AND	0 0 1 0	$Rd = Rs1 \& Rs2$
4	OR	0 0 1 1	$Rd = Rs1 Rs2$
5	NOT	0 1 0 0	$Rd = \sim Rs$
6	NOR	0 1 0 1	$Rd = Rs1 \sim Rs2$ If $Rs1 = Rs2$ Then $Equal = 1$, else $Equal = 0$ If $R1 = 0$ Then $AZ = 1$, else $AZ = 0$ If $Rs2 = 0$ Then $BZ = 1$, else $BZ = 0$ If $Rs1 > Rs2$ Then $AGB = 1$, else $AGB = 0$ If $Rs1 < Rs2$ Then $ALB = 1$, else $ALB = 0$
7	CMP (Equal)	0 1 1 0	$Rd = Rs1 \ll 1$
8	SHIFT LEFT	0 1 1 1	$Rd = Rs1 \gg 1$
9	SHIFT RIGHT	1 0 0 0	$Rd = Mem[Rs1]$
10	LOAD	1 0 0 1	$Mem[Rs1] = Rs2$
11	STORE	1 0 1 0	$PC = PC + Offset$
12	JUMP	1 0 1 1	No operation
13	NOP	1 1 0 0	$PC = PC + Offset$ if $Rd == 0$
14	JZ	1 1 0 1	$PC = PC + Offset$ if $Rd != 1$
15	JNZ	1 1 1 0	$Rd = 8\text{-bit Immediate}$
16	LOAD 8-BIT IMMEDIATE	1 1 1 1	

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