



FEATURES:

- Instruction set compatible with IDT79R3000A and RISCController Family MIPS RISC CPUs
- High level of integration minimizes system cost
 - RISC CPU
 - Multiply/divide unit
 - Instruction Cache
 - Data Cache
 - Programmable bus interface
 - Programmable port width support
- On-chip instruction and data caches
 - 2KB of Instruction Cache
 - 512B of Data Cache
- Flexible bus interface allows simple, low-cost designs
 - Superset pin-compatible with RISCController
 - Adds programmable port width interface (8-, 16-, and 32-bit memory sub-regions)
 - Adds programmable bus interface timing support (Extended address hold, Bus turn around time, Read/write masks)

- Double-frequency clock input
- 16.67MHz, 20MHz, 25MHz and 33MHz operation
- 20MIPS at 25MHz
- Low cost 84-pin PLCC packaging
- On-chip 4-deep write buffer eliminates memory write stalls
- On-chip 4-word read buffer supports burst or simple block reads
- On-chip DMA arbiter
- On-chip 24-bit timer
- Boot from 8-bit, 16-bit, or 32-bit wide PROMs
- Pin- and software-compatible family includes R3041, R3051, R3052™, and R3081™
- Complete software support
 - Optimizing compilers
 - Real-time operating systems
 - Monitors/debuggers
 - Floating Point emulation software
 - Page Description Languages

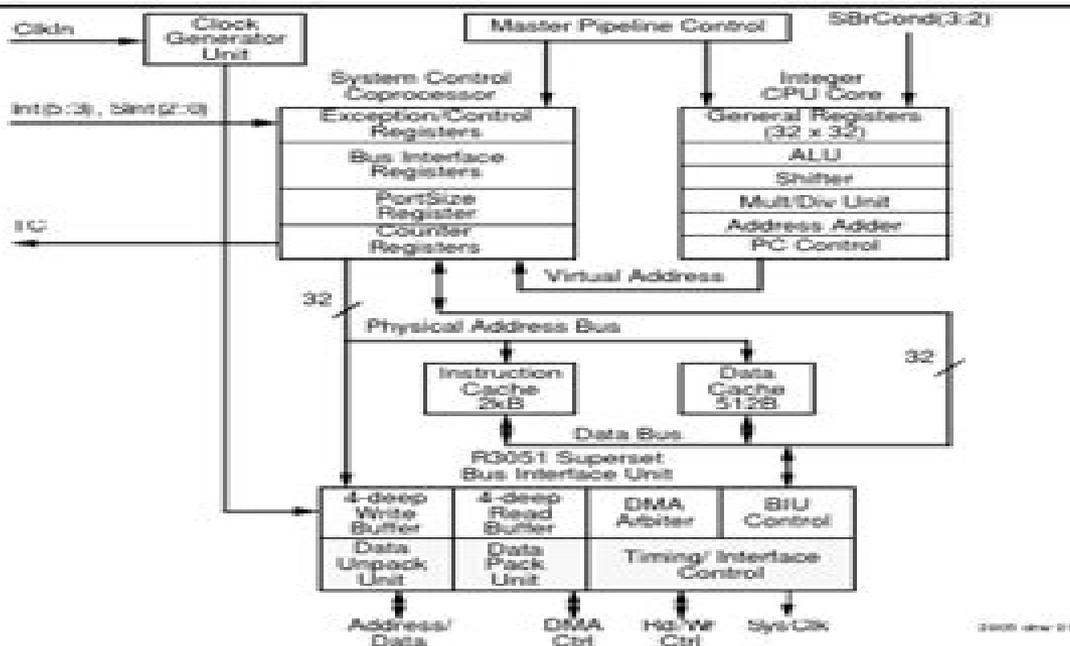


Figure 1. R3041 Block Diagram

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Integrated Device Idt79r3041 Hardware Guide User Guide

Christian Drosten



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